Hello people! I have a senior working in intel who got recruited from iitb. So according to him you need to focus on your digital basics, cmos working, TTL, and the king setup and hold time definition and how to avoid the violation etc. Be strongly prepared with your projects mentioned in your resume. And i told him that I haven't done ASIC flow he said no need to worry unless its mentioned in your CV. I Will try to get some interview questions as well and will share asap. Thats all for now. Good night

few important topics suggested by hemal shah:

clock domain crossing,two flop syncroniser,setup hold time fixing,,fixing timing violation after silicon production,blocking non blocking in verilig,modulo 1.5 ,3 counter

thorough with the projects mentioned in resume..

any updates regarding intel visit???????

Explain various adders and diff between them?

Explain the working of 4-bit Up/down Counter?

A circuit has 1 input X and 2 outputs A and B. If X = HIGH for 4 clock ticks, A = 1. If X = LOW for 4 clock ticks, B = 1. Draw a state diagram for this Spec?

Advantages and disadvantages of Mealy and Moore?

Id vs. Vds Characteristics of NMOS and PMOS transistors?

Explain the operation of a 6T-SRAM cell?

Differences between DRAM and SRAM?

Implement a function with both ratioed and domino logic and merits and demerits of each logic?

Given a circuit and asked to tell the output voltages of that circuit?

How can you construct both PMOS and NMOS on a single substrate?

What happens when the gate oxide is very thin?

What is setup time and hold time?

Write a pseudo code for sorting the numbers in an array?

What is pipelining and how can we increase throughput using pipelining?

Explain about stuck at fault models, scan design, BIST and IDDQ testing?

1. Insights of an inverter. Explain the working?  
   2. Insights of a 2 input NOR gate. Explain the working?  
   3. Insights of a 2 input NAND gate. Explain the working?  
   4. Implement F= not (AB+CD) using CMOS gates?  
   5. Insights of a pass gate. Explain the working?  
   6. Why do we need both PMOS and NMOS transistors to implement a pass gate?  
   7. What does the above code synthesize to?  
   8. Cross section of a PMOS transistor?  
   9. Cross section of an NMOS transistor?  
   10. What is a D-latch? Write the VHDL Code for it?  
   11. Differences between D-Latch and D flip-flop?  
   12. Implement D flip-flop with a couple of latches? Write a VHDL Code for a D flip-flop?  
   13. What is latchup? Explain the methods used to prevent it?  
   14. What is charge sharing?  
   15. While using logic design, explain the various steps that r followed to obtain the desirable design in a well defined manner?  
   16. Why is OOPS called OOPS? (C++)  
   17. What is a linked list? Explain the 2 fields in a linked list?  
   18. Implement a 2 I/P and gate using Tran gates?  
   19. Insights of a 4bit adder/Sub Circuit?  
   20. For f = AB+CD if B is S-a-1, what r the test vectors needed to detect the fault?  
   21. Explain various adders and diff between them?  
   22. Explain the working of 4-bit Up/down Counter?  
   23. A circuit has 1 input X and 2 outputs A and B. If X = HIGH for 4 clock ticks, A = 1. If X = LOW for 4 clock ticks, B = 1. Draw a state diagram for this Spec?  
   24. Advantages and disadvantages of Mealy and Moore?  
   25. Id vs. Vds Characteristics of NMOS and PMOS transistors?  
   26. Explain the operation of a 6T-SRAM cell?  
   27. Differences between DRAM and SRAM?  
   28. Implement a function with both ratioed and domino logic and merits and demerits of each logic?  
   29. Given a circuit and asked to tell the output voltages of that circuit?  
   30. How can you construct both PMOS and NMOS on a single substrate?  
   31. What happens when the gate oxide is very thin?  
   32. What is setup time and hold time?  
   33. Write a pseudo code for sorting the numbers in an array?  
   34. What is pipelining and how can we increase throughput using pipelining?  
   35. Explain about stuck at fault models, scan design, BIST and IDDQ testing?  
   36. What is SPICE?  
   37. Differences between IRSIM and SPICE?  
   38. Differences between netlist of HSPICE and Spectre?  
   39. What is FPGA?  
   40. Draw the Cross Section of an Inverter? Clearly show all the connections between M1 and poly, M1 and diffusion layers etc?  
   41. Draw the Layout of an Inverter?  
   42. If the current thru the poly is 20nA and the contact can take a max current of 10nA how would u overcome the problem?  
   43. Implement F = AB+C using CMOS gates?  
   44. Working of a 2-stage OPAMP?  
   45. 6-T XOR gate?  
   46. Differences between blocking and Non-blocking statements in Verilog?  
   47. Differences between Signals and Variables in VHDL? If the same code is written using Signals and Variables what does it synthesize to?  
   48. Differences between functions and Procedures in VHDL?  
   49. What is component binding?  
   50. What is polymorphism? (C++)  
   51. What is hot electron effect?  
   52. Define threshold voltage?  
   53. Factors affecting Power Consumption on a chip?  
   54. Explain Clock Skew?  
   55. Why do we use a Clock tree?  
   56. Explain the various Capacitances associated with a transistor and which one of them is the most prominent?  
   57. Explain the Various steps in Synthesis?  
   58. Explain ASIC Design Flow?  
   59. Explain Custom Design Flow?  
   60. Why is Extraction performed?  
   61. What is LVS, DRC?  
   62. Who provides the DRC rules?  
   63. What is validation?  
   64. What is Cross Talk?  
   65. Different ways of implementing a comparator?  
   66. What r the phenomenon which come into play when the devices are scaled to the sub-micron lengths?  
   67. What is clock feed through?  
   68. Implement an Inverter using a single transistor?  
   69. What is Fowler-Nordheim Tunneling?  
   70. Insights of a Tri-state inverter?  
   71. If an/ap = 0.5, an/ap = 1, an/ap = 3, for 3 inverters draw the transfer characteristics?  
   72. Differences between Array and Booth Multipliers?  
   73. Explain the concept of a Clock Divider Circuit? Write a VHDL code for the same?  
   74. Which gate is normally preferred while implementing circuits using CMOS logic, NAND or NOR? Why?  
   75. Insights of a Tri-State Inverter?  
   76. Basic Stuff related to Perl?  
   77. Have you studied buses? What types?  
   78. Have you studied pipelining? List the 5 stages of a 5 stage pipeline. Assuming 1 clock per stage, what is the latency of an instruction in a 5 stage machine? What is the throughput of this machine ?  
   79. How many bit combinations are there in a byte?  
   80. For a single computer processor computer system, what is the purpose of a processor cache and describe its operation?  
   81. Explain the operation considering a two processor computer system with a cache for each processor.  
   82. What are the main issues associated with multiprocessor caches and how might you solve them?  
   83. Explain the difference between write through and write back cache.  
   84. Are you familiar with the term MESI?  
   85. Are you familiar with the term snooping?  
   86. Describe a finite state machine that will detect three consecutive coin tosses (of one coin) that results in heads.  
   87. In what cases do you need to double clock a signal before presenting it to a synchronous state machine?  
   88. You have a driver that drives a long signal & connects to an input device. At the input device there is either overshoot, undershoot or signal threshold violations, what can be done to correct this problem?  
     
   92. Are you familiar with VHDL and/or Verilog?  
   93. What types of CMOS memories have you designed? What were their size? Speed?  
   94. What work have you done on full chip Clock and Power distribution? What process technology and budgets were used?  
   95. What types of I/O have you designed? What were their size? Speed? Configuration? Voltage requirements?  
   96. Process technology? What package was used and how did you model the package/system? What parasitic effects were considered?  
   97. What types of high speed CMOS circuits have you designed?  
   98. What transistor level design tools are you proficient with? What types of designs were they used on?  
   99. What products have you designed which have entered high volume production?  
   100. What was your role in the silicon evaluation/product ramp? What tools did you use?  
   101. If not into production, how far did you follow the design and why did not you see it into production?